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09/589,716	06/08/2000	Stephen V. Kosonocky	YO999-369	9798

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/589,716	Applicant(s) KOSONOCKY, STEPHEN V.
	Examiner Chat C. Do	Art Unit 2124

-- Th MAILING DATE of this communication appears on th cov r sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/14/2003; 11/12/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This communication is responsive to Amendment B, filed 10/14/2003.

2. Claims 1-20 are pending in this application. Claims 1, 6, 13, and 20 are independent claims. In Amendment B, claims 1, 6, 13, and 20 are amended. This action is made non-final after a Request for Continued Examination filed.

Claim Objections

3. Claim 18 is objected to because of the following informalities: a period (.) is required at the end of claim 18 line 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification fails to disclose the whole invention wherein the binary output signal S(n) is implemented in accordance with an expression: S(n) = ^(p(n) * C(n-1)) * (p(n) + C(n-1)). The whole invention is mapped into Figure 1 as a dynamic logic adder,

however, the dynamic logic adder is implemented according to this expression instead:

$S(n) = \wedge[\{p(n)*C(n-1)\} + \wedge\{p(n) + C(n-1)\}]$.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. 5,905,667).

Re claim 1, Lee discloses an apparatus for use in summing at least two binary values (A and B) in Figure 3 comprising a binary adder circuit respective to a first binary value (A) a second binary value (B) and a carry value (C) and operative to generate a binary output value (SUM) representative of a summation of the first binary value the second binary value and the carry value the binary adder circuit having dynamic logic (abstract), without inversion of signals driving one or more dynamic nodes associated with the dynamic logic (no inverter or inverting mechanism is used in Figure 3), for implement an exclusive OR function (MP33, MP34 and col. 1 lines 41-45) that generates the binary output value (SUM) without one of a positive and a negative complementary version of the carry value (only C is applied to 31 and 33).

Re claim 3, Lee further discloses the logic of the binary adder circuit in Figure 3 comprising a first NMOS transistor stage (left portion of 31) for performing an AND

operation on the generate signal (C) and the propagate signal (parallel NMOS A and B); an inverter stage (MP31), coupled to the first NMOS transistor stage for inverting an output signal generated by the first NMOS transistor stage (CARRY'); a second NMOS transistor stage (left lower portion of 33 wherein A, B, and C are structured in parallel) for performing an OR operation on the generate signal (C) and the propagate signal (parallel NMOS and B); and a NOR gate (other portion of 33 and 34), coupled to the inverter stage (31) and the second NMOS transistor stage (left lower portion of 33), for combining an output signal generated by the inverter stage and an output signal generated by the second NMOS transistor stage to generate the binary output value.

Re claim 4, Lee further discloses in Figure 3 the first NMOS transistor stage is responsive to more than one generate signal (C) and more than one propagate signal (A and B).

Re claim 5, Lee further discloses in Figure 3 the second NMOS transistor stage is responsive to more than one generate signal (C) and more than one propagate signal (A and B).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being obvious over Suzuki (U.S. 3,646,332) in view of Lee (U.S. 5,905,667).

Re claim 1, Suzuki discloses an apparatus for use in summing at least two binary values (binary A and B) in Figures 4 and 8 comprising a binary adder circuit (Figure 8) responsive to a first binary value (A), a second binary value (B), and a carry value (C or output of 5) and operative to generate a binary output value (S or sum or output of 12) representative of a summation of the first binary value the second binary value and the carry value the binary adder circuit having logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic (no inverter or inverting mechanism is used in Figure 3), for implement an exclusive OR function (2' with Figure 4 as the logical structure of EXOR and col. 3 lines 16-20) that generates the binary output value without one of appositive and a negative complementary version of the carry value (only C is inputted to component 2' to compute the sum). Suzuki does not disclose the adder is using a dynamic logic. However, the dynamic logic is well-known in the art as used in Lee's invention. Lee discloses the dynamic logics (abstract) to compute a binary addition. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the dynamic logic as disclosed in Lee's invention into Suzuki's invention because it would enable to reduce the power consumption and increase the system performance.

10. Claims 6-9, 11-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being obvious by Jiang et al. (U.S. 5,943,251) in view of Lee (U.S. 5,905,667).

Re claim 6, Jiang et al. disclose a N-bit parallel adder (col. 8 line 10) in Figure 7 comprising: a first logic stage configured to receive a first N-bit binary value and a second N-bit binary value and compute generate signals and propagate signals for each bit (P0G0-P35G35); a second logic stage coupled to the first logic stage (30-38) configured to compute block generate signal ($G^4_0 - G^4_8$) and block propagate signals ($P^4_0 - P^4_8$) for groups of one through m (m = 9) bits from the generate (G0-G35) and propagate (P0-P35) signals computed in the first logic stage; a third logic stage (40-42) coupled to the second logic stage (30-38) configured to combine the block generate and block propagate signals of one set of groups with the block generate ($G^{12}_0 - G^{12}_0$) and block propagate signals of another set of groups ($P^{12}_0 - P^{12}_0$); and a fourth logic stage (40) coupled to the third logic stage (40-42) configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal (Figure 8) wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation (Figure 7 and equations 3-7 in col. 1), wherein at least one of the logic stages has dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Jiang does not disclose the adder is using a dynamic logic. However, the dynamic logic is well-known in the art as used in Lee's invention. Lee discloses the dynamic logics (abstract) to compute a binary addition. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the dynamic logic as disclosed in Lee's

invention into Jiang's invention because it would enable to reduce the power consumption and increase the system performance.

Re claim 7, Jiang et al. further disclose a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i (col. 2 line 43), wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$ where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i (col. 1 equation 1) where a represents the first binary value and b represents the second binary value, and where p represents the propagate signal (col. 1 equation 2) and is equivalent to a logical summation operation between a_i and b_i.

Re claim 8, Jiang et al. further disclose in Figure 7 the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals (equation 7 in col. 1 wherein Ci is in col. 2 line 43).

Re claim 9, Jiang et al. further discloses in Figure 7 the fourth logic stage implements an exclusive OR function to generate the summation signal (col. 4 lines 16-17).

Re claim 11, Jiang et al. further disclose N is equal to 64 (col. 8 line 10 N = 64).

Re claim 13, it is the method claim of claim 6. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 12, Jiang et al. do not disclose the logic stages are implemented with complementary metal oxide semiconductor components. However, Lee discloses in Figure 3 the logic stages are implemented with complementary metal oxide semiconductor components (31). Therefore, it would have been obvious to a person

having ordinary skill in the prior art at the time the invention is made to implement the logic stages disclosed by Jiang et al. with complementary metal oxide semiconductor components because it would enable to generate the complemented signal for computing the sum of two or more binary numbers and reduce the power consumption (col. 1 lines 37-42).

Re claim 14, it is the method claim of claim 7. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 15, it is the method claim of claim 8. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 16, it is the method claim of claim 9. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 18, it is the method claim of claim 11. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 19, it is the method claim of claim 12. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 12.

Re claim 20, it is the device claim of claim 6. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 6.

Response to Arguments

11. Applicant's arguments filed 10/14/2003 have been fully considered but they are not persuasive.

a. The applicant argues in page 7 fourth paragraph for the rejection of claims 1-20 under 35 U.S.C. 112 first paragraph to be withdrawn because the expressions for binary output signal S(n) in the final Office Action is equivalent to the expression in the current specification.

The examiner does not quite understand the argument that is pointed out by the applicant. However, Figure 1 discloses an adder circuit that is not implemented in accordance with an expression in claim 2 wherein Figure 1 circuit requires 2 complementary version of signals as S(n) = ^[{p(n)*C(n-1)} + ^{p(n) + C(n-1)}]. The expression in claim 2 only requires 1 complementary version of signal as S(n) = ^(p(n) * C(n-1)) * (p(n) + C(n-1)). Therefore, the rejection

b. The applicant argues in page 8 second paragraph for claim 1 that the cited reference by Lee discloses the inversion of signals driving one or more dynamic nodes associated with the dynamic logic through the inversion of its CARRY and SUM signals.

The examiner respectfully submits that claim 1 does not specific without inversion of signals through the inversion of its CARRY and SUM signals.

Second, both Figures 1 and 4 (part d17 and d18 in Figure 1; parts 86 and 88 in Figure 4) of the present application disclose the inversion of signals driving one or more dynamic nodes associated with the dynamic logic through the inversion of its SUM signals.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

January 13, 2004

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100